Application No.: 10/788,913
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**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Original) A method of driving an SRAM-compatible memory including memory blocks and sense amplifiers, the memory blocks each having DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory externally interfacing with an external system in which no timing period for performing a refresh operation is provided and first and second external access periods are provided for externally accessing the SRAM-compatible memory, the first external access period including a first refresh period and a first internal access period and the second external access period including a second refresh period, the method comprising the steps of:

a) fetching data to be refreshed from a DRAM cell in a first row of a first memory block and storing the fetched data in a first sense amplifier during the first refresh period;

b) storing the data fetched from the DRAM cell in the first row of the first memory block and stored in the first sense amplifier in a second sense amplifier;

c) storing data accessed from a DRAM cell in a second row of the first memory block in the first sense amplifier during the first internal access period; and

d) rewriting the data stored in the second sense amplifier in the DRAM cell in the first row of the first memory block during the second refresh period.

2. (Original) The method according to claim 1, further comprising the step of reading the data which is stored in the first sense amplifier in the step c) to an outside of the first sense amplifier.

3. (Currently Amended) The method according to claim 1, further comprising the step of writing the data which is stored in the ~~second~~ first sense amplifier in the ~~step b)~~ step c) in the DRAM cell in the second row of the first memory block.

4. (Original) The method according to claim 1, wherein the step b) is performed during the first refresh period.

5. (Original) The method according to claim 1, wherein the step b) is performed in response to an address signal for selecting the second row of the first memory block.

6. (Cancelled)

7. (Currently Amended) The method of claim ~~1~~6, further comprising the steps of:

storing the data fetched in the step a) in a sense amplifier of the memory block; and

reading the data stored in ~~the sense amplifier~~ a sense amplifier outside the memory block during the first internal access period.

8. (Original) A method of driving an SRAM-compatible memory including memory blocks and sense amplifiers, the memory blocks each having DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory externally interfacing with an external system in which no timing period for performing a refresh operation is provided and first and second external access periods are provided for externally accessing the SRAM-compatible memory, the first external access period including a first refresh period and a first internal access period and the second external access period including a second refresh period, the method comprising the steps of:

a) fetching first data to be refreshed from a DRAM cell in a first row of a first memory block and storing the fetched first data in a first sense amplifier during the first refresh period;

b) fetching second data from a DRAM cell in a first row of a second memory block and storing the fetched second data in a second sense amplifier during the first internal access period; and

c) rewriting the first data amplified by and stored in the first sense amplifier in the DRAM cell in the first row of the first memory block during the second refresh period.

9. (Original) The method according to claim 8, further comprising the step of reading the fetched second data which is stored in the second sense amplifier in the step b) to an outside of the second sense amplifier.

10. (Original) An SRAM-compatible memory device including DRAM cells arranged in a matrix form defined by rows and columns, and externally interfacing with an external system in which no timing period is provided for performing a refresh operation of the DRAM cells, the SRAM-compatible memory device comprising:

first and second memory blocks each having the DRAM cells;

a first sense amplifier for amplifying and latching data fetched from a DRAM cell in the first memory block;

a second sense amplifier for amplifying and latching data fetched from a DRAM cell in the second memory block;

a first switching unit for controlling an electrical connection of data input/output lines between the first memory block and the first sense amplifier;

a second switching unit for controlling an electrical connection of data input/output lines between the second memory block and the second sense amplifier; and

a third switching unit for controlling an electrical connection between the first and second sense amplifiers.

11. (Original) The SRAM-compatible memory device according to claim 10, further comprising:

a first equalizing unit for equalizing the data input/output lines of the first memory block; and

a second equalizing unit for equalizing the data input/output lines of the second memory block.

12. (Original) The SRAM-compatible memory device according to claim 10, wherein first and second external access periods are provided for externally accessing the SRAM-compatible memory device, the first external access period including a first refresh period and a first internal access period and the second external access period including a second refresh period, the first switching unit transmitting data fetched from a DRAM cell in a first row of the first memory block to the first sense amplifier during the first refresh period.

13. (Original) The SRAM-compatible memory device according to claim 12, wherein the third switching unit transmits the data fetched from the DRAM cell in the first row of the first memory block and stored in the first sense amplifier to the second sense amplifier during the first refresh period.

14. (Original) The SRAM-compatible memory device according to claim 13, wherein the data stored in the second sense amplifier is read out and rewritten in the DRAM cell in the first row of the first memory block during the second refresh period.

15. (Original) The SRAM-compatible memory device according to claim 10, wherein the first switching unit transmits data fetched from a DRAM cell in a second row of the first memory block to the first sense amplifier during the first internal access period.

16. (Original) An SRAM-compatible memory device including memory blocks each having DRAM cells arranged in a matrix form defined by rows and columns, and externally interfacing with an external system in no timing period is provided for performing a refresh operation of the DRAM cells, the SRAM-compatible memory device comprising:

first and second memory blocks each having DRAM cells which are accessed by being specified by input addresses, access operations of the DRAM cells being independent of each other;

a first sense amplifier for amplifying and latching data fetched from an accessed DRAM cell in the first memory block during a normal access operation;

a second sense amplifier for amplifying and latching data fetched from an accessed DRAM cell in the second memory block during the normal access operation;

a first switching unit for controlling an electrical connection of data input/output lines between the first memory block and the first sense amplifier;

a second switching unit for controlling an electrical connection of data input/output lines between the second memory block and the second sense amplifier; and

a third switching unit for controlling an electrical connection between the first and second sense amplifiers.

17. (Original) The SRAM-compatible memory device according to claim 16, wherein:

the SRAM-compatible memory device performs a predetermined external access operation during an external access period, the external access period including a refresh period and an internal access period in sequence;

the first switching unit transmits data fetched from a DRAM cell in a first row of the first memory block to the first sense amplifier during the refresh period; and

the third switching unit transmits the data fetched from the DRAM cell in the first row and stored in the first sense amplifier to the second sense amplifier and latches the transmitted data therein, when a DRAM cell in a second row of the first memory block is specified.

18. (Cancelled)